Features

- Low-voltage and standard-voltage operation
  - V_{CC} = 1.7V to 5.5V
- User-selectable internal organization
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- Three-wire serial interface
- Sequential read operation
- 2MHz clock rate (5V)
- Self-timed write cycle (5ms max)
- High reliability
  - Endurance: One million write cycles
  - Data retention: 100 years
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, and 8-ball VFBGA packages

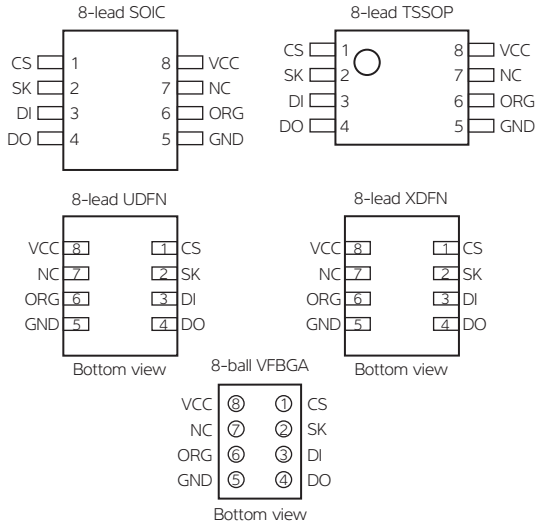
Description

The Atmel® AT93C56B/66B provides 2048/4096 bits of serial electrically erasable programmable read-only memory (EEPROM) organized as 128/256 words of 16 bits each (when the ORG pin is connected to V_{CC}) and 256/512 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C56B/66B is available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, and 8-ball VFBGA packages.

The AT93C56B/66B is enabled through the chip select pin (CS) and accessed via a three-wire serial interface consisting of data input (DI), data output (DO), and shift clock (SK). Upon receiving a read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin, DO. The write cycle is completely self-timed, and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the erase/write enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the ready/busy status of the part.

The AT93C56B/66B operates from 1.7V to 5.5V.

Figure 0-1. Pin Configurations



Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
NC	No Connect

Three-wire Serial Electrically Erasable Programmable Read-only Memory

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Atmel AT93C56B
Atmel AT93C66B

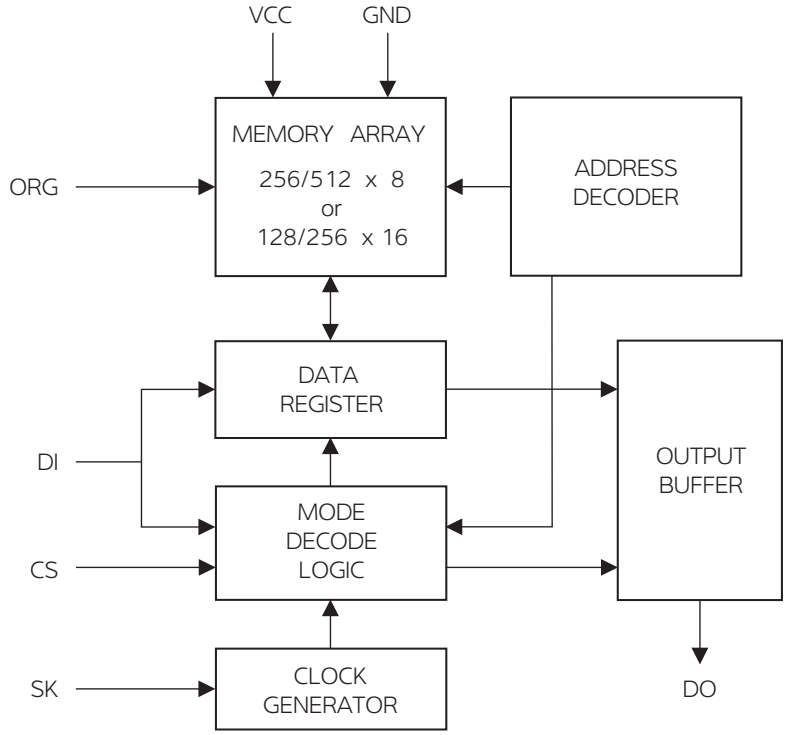
8735A–SEEPR–1/11

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram



Note: When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1MΩ pull-up resistor, then the x 16 organization is selected.

Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Notes: 1. This parameter is characterized, and is not 100% tested

Table 1-2. DC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.7		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0MHz		0.5	2.0	mA
			WRITE at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
V_{IL1}[1] V_{IH1}[1]	Input Low Voltage Input High Voltage	2.5V ≤ V_{CC} ≤ 5.5V		–0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}[1] V_{IH2}[1]	Input Low Voltage Input High Voltage	1.7V ≤ V_{CC} ≤ 2.5V		–0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	2.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1mA			0.4	V
			I_{OH} = –0.4mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.7V ≤ V_{CC} ≤ 2.5V	I_{OL} = 0.15mA			0.2	V
			I_{OH} = –100µA	V_{CC} – 0.2			V

Notes: 1. V_{IL} min and V_{IH} max are reference only, and are not tested

Table 1-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, V_{CC} = as specified, CL = 1 TTL gate and 100pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$		0 0 0		2 1 0.25	MHz
t_{SKH}	SK High Time	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$		250 1000			ns
t_{SKL}	SK Low Time	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$		250 1000			ns
t_{CS}	Minimum CS Low Time	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$		250 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$	50 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$	100 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$	100 400			ns
t_{PD1}	Output Delay to 1	AC Test	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$			250 1000	ns
t_{PD0}	Output Delay to 0	AC Test	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$			250 1000	ns
t_{SV}	CS to Status Valid	AC Test	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$			250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$2.5V \le V_{CC} \le 5.5V$ $1.7V \le V_{CC} \le 5.5V$			150 400	ns
t_{WP}	Write Cycle Time		$1.7V \le V_{CC} \le 5.5V$			5	ms
Endurance[1]	5.0V, 25°C			1,000,000			Write Cycles

Notes: 1. This parameter is characterized, and is not 100% tested

Table 1-4. Instruction Set for the Atmel AT93C56B and Atmel AT93C66B

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	$A_8 - A_0$	$A_7 - A_0$			Reads data stored in memory at specified address
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes
ERASE	1	11	$A_8 - A_0$	$A_7 - A_0$			Erases memory location $A_n - A_0$
WRITE	1	01	$A_8 - A_0$	$A_7 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Writes memory location $A_n - A_0$
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V
WRAL	1	00	01XXXXXXX	01XXXXXX	$D_7 - D_0$	$D_{15} - D_0$	Writes all memory locations. Valid only at V_{CC} = 5.0V ±10% and disable register cleared
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions

Note: The Xs in the address field represent "don't care" values, and must be clocked

2. Functional Description

The Atmel® AT93C56B/66B is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. **A valid instruction starts with a rising edge of CS**, and consists of a start bit (logic one) followed by the appropriate op code and the desired memory address location.

READ (READ): The read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin, DO. Output data changes are synchronized with the rising edges ofthe serial clock, SK. It should be noted that a dummy bit (logic zero) precedes the 8- or 16-bit data output string. The AT93C56B/66B supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as chip select (CS) is held high. In this case, the dummy bit (logic zero) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

ERASE/WRITE ENABLE (EWEN): To assure data integrity, the part automatically goes into the erase/write disable (EWDS) state when power is first applied. An erase/write enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The erase (ERASE) instruction programs all bits in the specified memory location to the logical-one state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A logic one at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8- or 16-bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A logic zero at DO indicates that programming is still in progress. A logic one indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. **A ready/busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle, t_{WP}.**

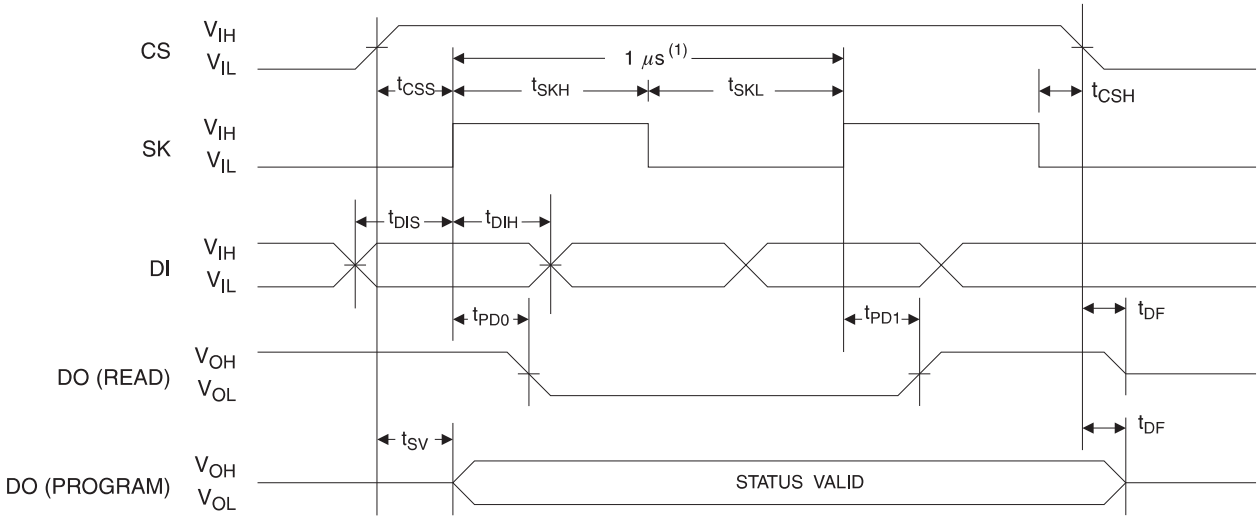
ERASE ALL (ERAL): The erase all (ERAL) instruction programs every bit in the memory array to the logic one state, and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The write all (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturbance, the erase/write disable (EWDS) instruction disables all programming modes, and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions, and can be executed at any time.

3. Timing Diagrams

Figure 3-1. Synchronous Data Timing



Note: 1. This is the minimum SK period

Table 3-1. Organization Key for Timing Diagrams

I/O	Atmel AT93C56B (2K)		Atmel AT93C66B (4K)	
	x 8	x 16	x 8	x 16
A_N	A_8 (1)	A_7 (2)	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}

Notes: 1. A_8 is a don't-care value, but the extra clock is required
2. A_7 is a don't-care value, but the extra clock is required

Figure 3-2. READ Timing

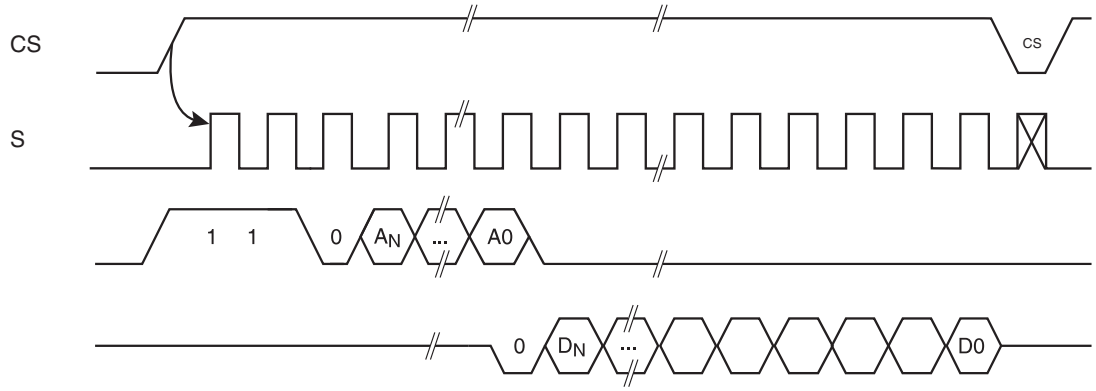


Figure 3-3. EWEN Timing

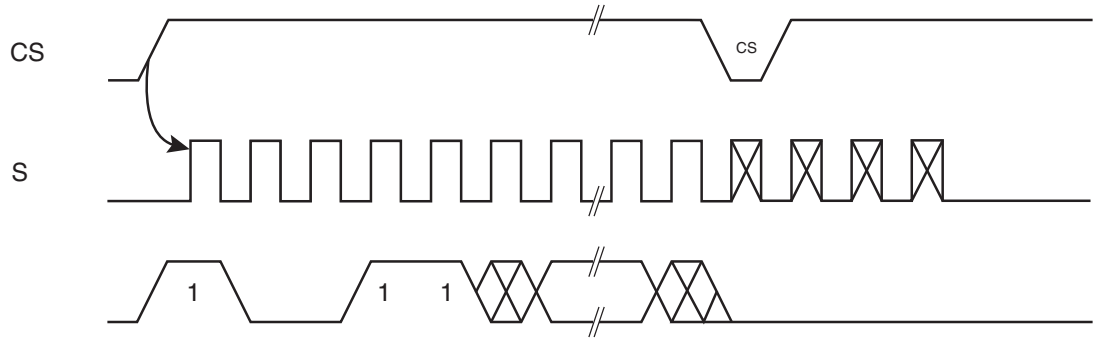


Figure 3-4. EWDS Timing

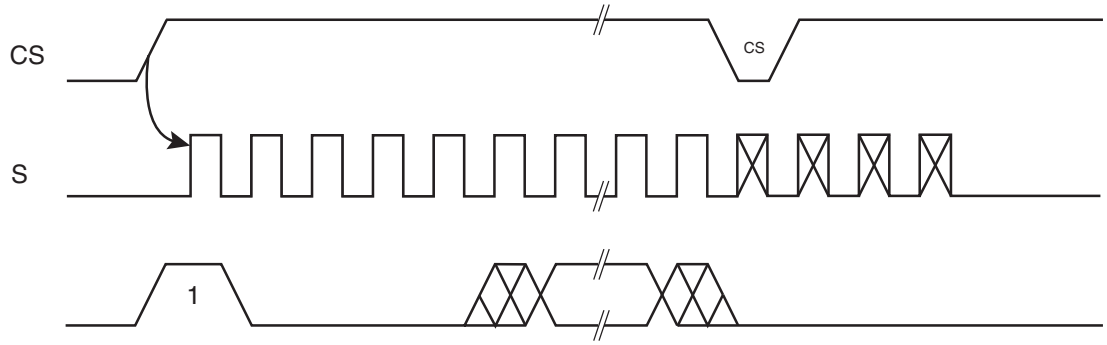


Figure 3-5. WRITE Timing

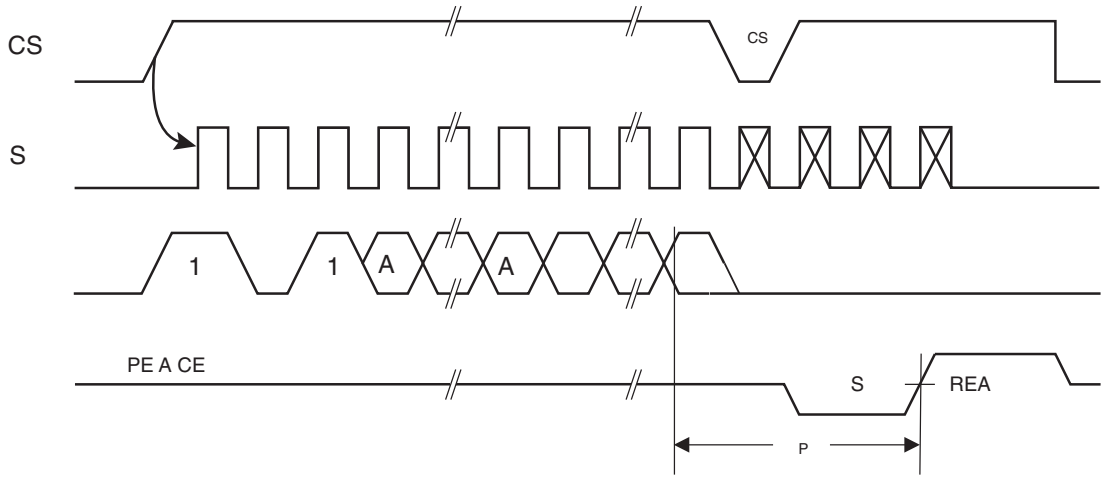
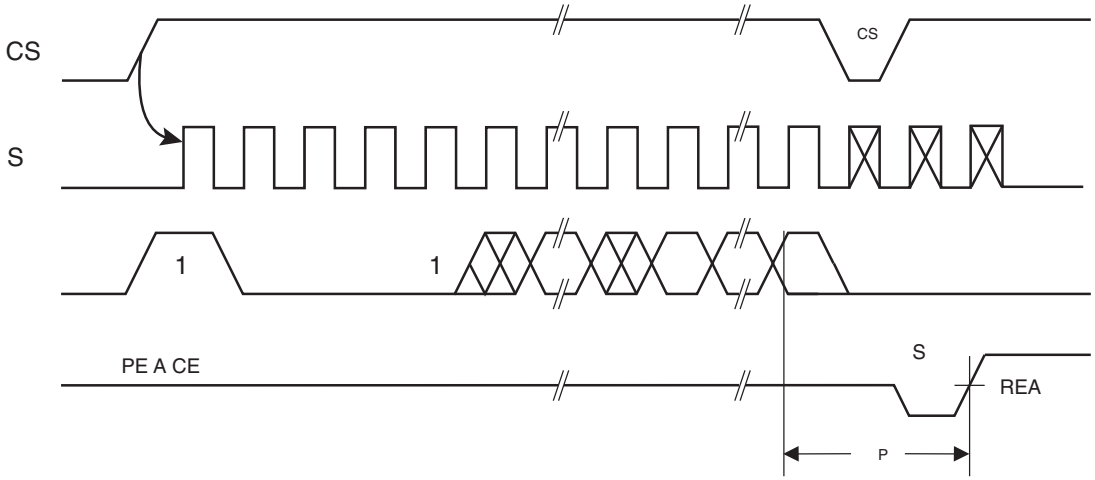


Figure 3-6. WRAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V

Figure 3-7. ERASE Timing

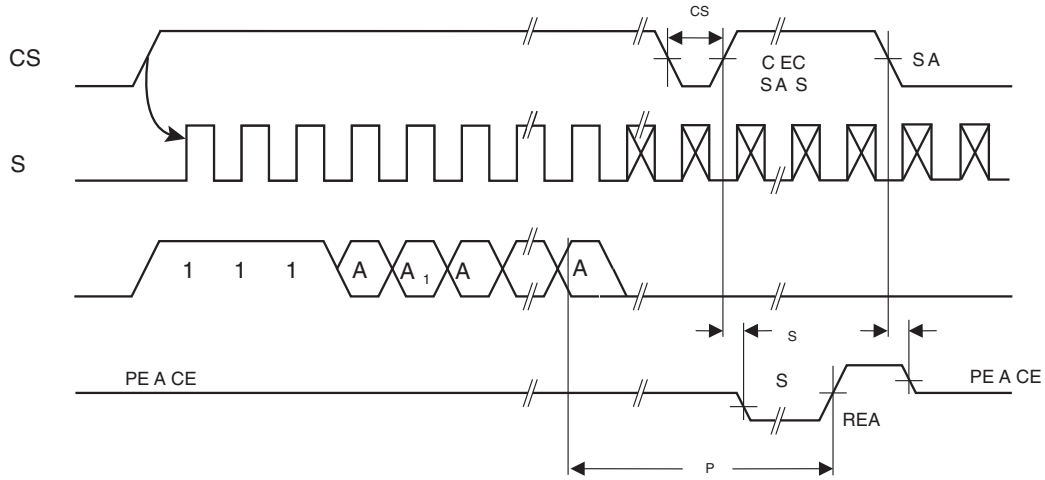
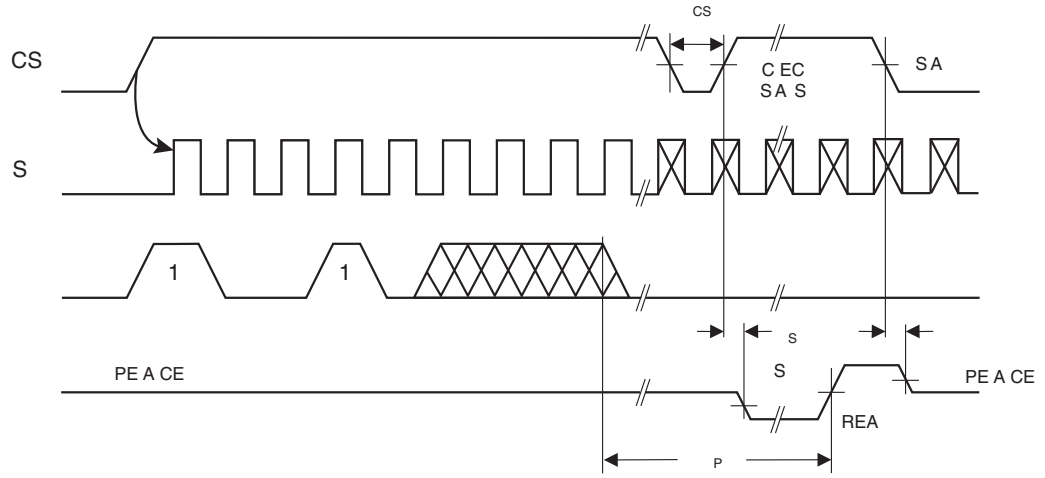
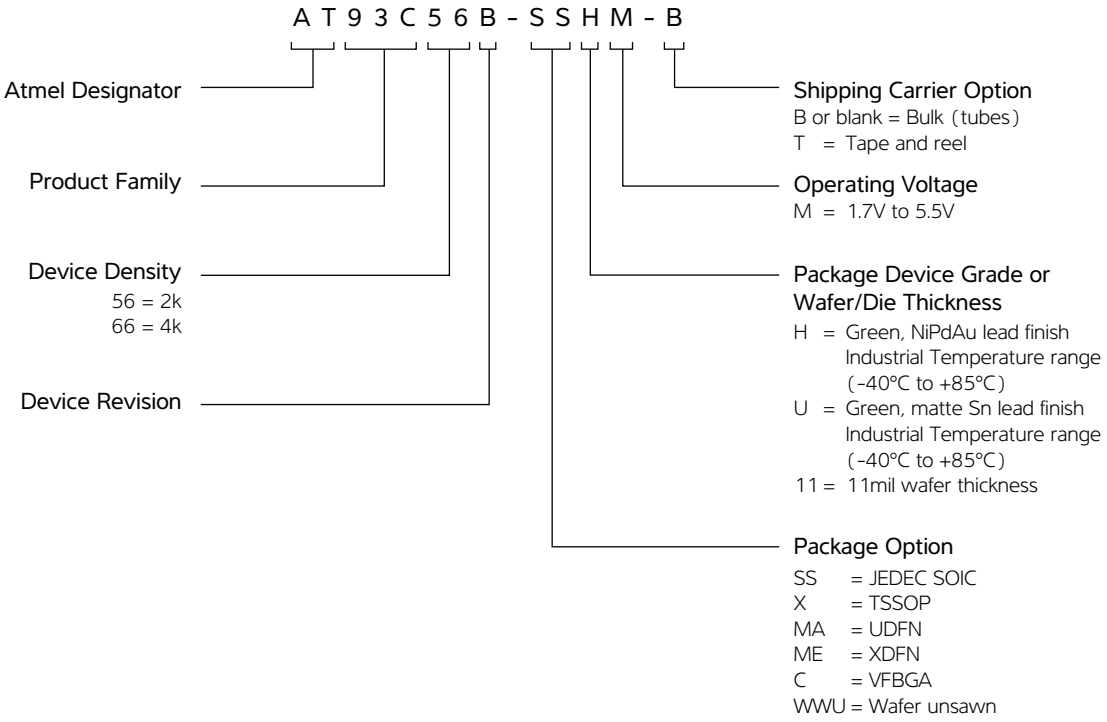


Figure 3-8. ERAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V

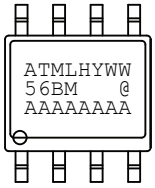
4. Ordering Code Detail



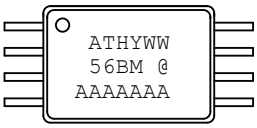
5. Part Markings

5.1 Atmel AT93C56B

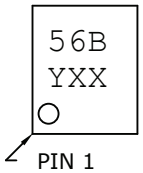
8 lead SOIC
3 Rows of 8 Characters



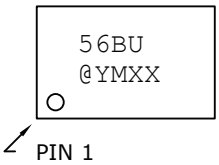
8 lead TSSOP
3 Rows
2 of 6 and 1 of 7 Characters



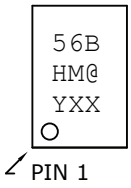
8 lead XDFN - 1.8x2.2mm
2 Rows of 3 Characters



8-ball VFBGA - 2.35x3.73mm
2 Rows
1 of 4 and 1 of 5 Characters



8 lead UDFN -2.0x3.0mm
3 Rows of 3 Characters



Catalog Number: AT93C56B Catalog Truncation: 56B

Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	Blank: 2.7v min
0: 2010 4: 2014	A: January	02: Week 2	D: 2.5v min
1: 2011 5: 2015	B: February	04: Week 4	L: 1.8v min
2: 2012 6: 2016	" " "	" " "	M: 1.7v min
3: 2013 7: 2017	L: December	52: Week 52	P: 1.5v min
Trace Code			Grade/Lead Finish Material
XX = Trace Code (ATMEL Lot Numbers to Correspond to Code) (e.g. XX: AA, AB...YZ, ZZ)			U: Industrial/Matt Tin H: Industrial/NiPdAu
Lot Number			
AAAAAAA = ATMEL Wafer Lot Number			ATMEL Truncation
Country of Assembly			AT: ATMEL
@ = Country of Assembly B = PHILIPPINES W = THAILAND Q = MALAYSIA H,Y = CHINA			ATM: ATMEL ATML: ATMEL

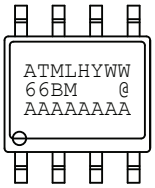
1/12/11

Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE **93C56BSM**, AT93C56B Standard Marking Information for Package Offering	DRAWING NO. 93C56BSM	REV. A

5.2 Atmel AT93C66B

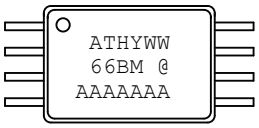
8 lead SOIC

3 Rows of 8 Characters



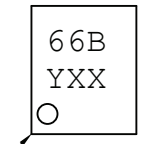
8 lead TSSOP

3 Rows
2 of 6 and 1 of 7 Characters



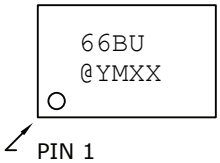
8 lead XDFN - 1.8x2.2mm

2 Rows of 3 Characters



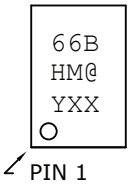
8-ball VFBGA - 2.35x3.73mm

2 Rows
1 of 4 and 1 of 5 Characters



8 lead UDFN - 2.0x3.0mm

3 Rows of 3 Characters



Catalog Number: AT93C66B Catalog Truncation: 66B

Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	Blank: 2.7v min
0: 2010 4: 2014	A: January	02: Week 2	D: 2.5v min
1: 2011 5: 2015	B: February	04: Week 4	L: 1.8v min
2: 2012 6: 2016	" " "	" " "	M: 1.7v min
3: 2013 7: 2017	L: December	52: Week 52	P: 1.5v min
Trace Code			Grade/Lead Finish Material
XX = Trace Code (ATMEL Lot Numbers to Correspond to Code) (e.g. XX: AA, AB...YZ, ZZ)			U: Industrial/Matt Tin H: Industrial/NiPdAu
Lot Number			
AAAAAAA = ATMEL Wafer Lot Number			ATMEL Truncation
Country of Assembly			AT: ATMEL ATM: ATMEL ATML: ATMEL
@ = Country of Assembly B = PHILIPPINES W = THAILAND Q = MALAYSIA H,Y = CHINA			

1/12/11

Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	93C66BSM, AT93C66B Standard Marking Information for Package Offering	93C66BSM	A

5.3 Atmel AT93C56B Ordering Information

Atmel Ordering Code	Voltage	Package	Operation Range
AT93C56B-SSHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	Lead-free/Halogen-free/ Industrial Temperature (−40°C to 85°C)
AT93C56B-SSHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	
AT93C56B-XHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT93C56B-XHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT93C56B-MAHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8Y6	
AT93C56B-MEHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8ME1	
AT93C56B-CUM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8U3-1	
AT93C56B-WWU11M	1.7 to 5.5	Die Sale	Industrial Temperature (−40°C to 85°C)

Notes:
1. "-B" denotes bulk delivery
2. "-T" denotes tape and reel delivery. SOIC = 4k/reel. TSSOP UDFN, XDFN, and VFBGA = 5k/reel
3. For wafer sales, please contact Atmel sales

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing, Small OutlinePackage (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Dual No Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body (XDFN)
8U3-1	8-ball, 1.50mm x 2.00mm Body, 0.50mm Pitch, Small Die Ball Grid Array (VFBGA)

5.4 Atmel AT93C66B Ordering Information

Atmel Ordering Code	Voltage	Package	Operation Range
AT93C66B-SSHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT93C66B-SSHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	
AT93C66B-XHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT93C66B-XHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT93C66B-MAHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8Y6	
AT93C66B-MEHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8ME1	
AT93C66B-CUM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8U3-1	
AT93C56B-WWU11M	1.7 to 5.5	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes: 1. "-B" denotes bulk delivery
2. "-T" denotes tape and reel delivery. SOIC = 4k/reel. TSSOP UDFN, XDFN, and VFBGA = 5k/reel
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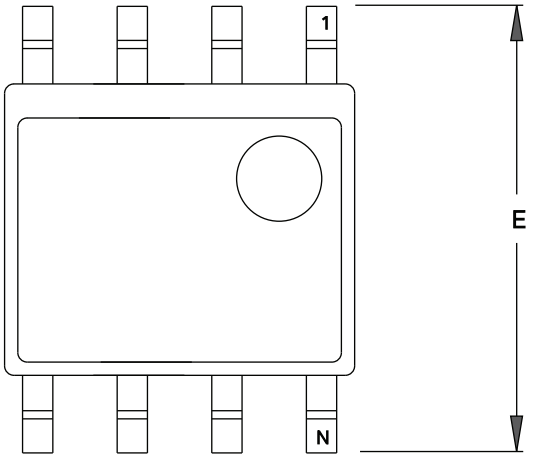
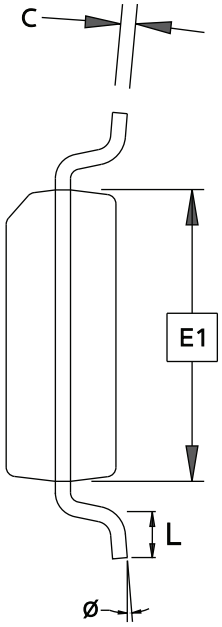
8U3-1	8-ball, 1.50mm x 2.00mm Body, 0.50mm Pitch, Small Die Ball Grid Array (VFBGA)

6. Packaging Information

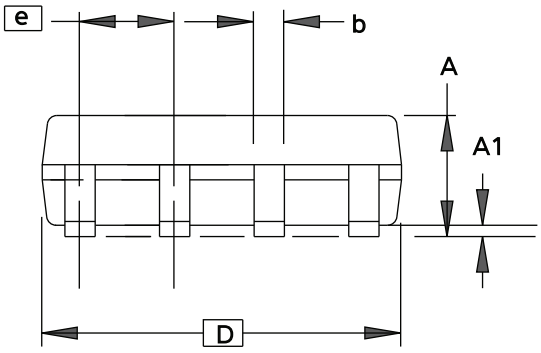
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

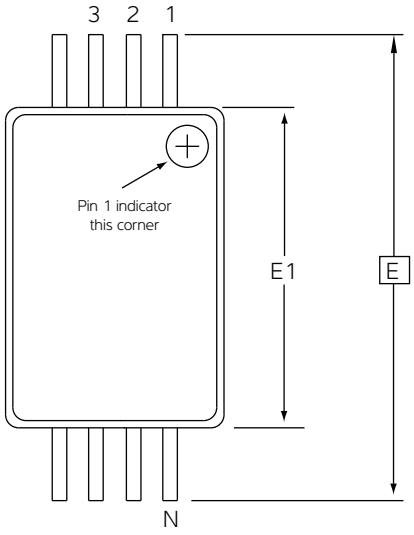
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

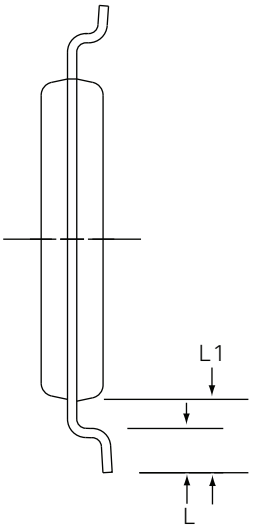
5/19/10

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	F

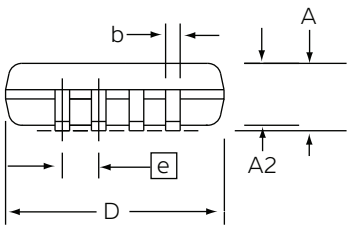
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

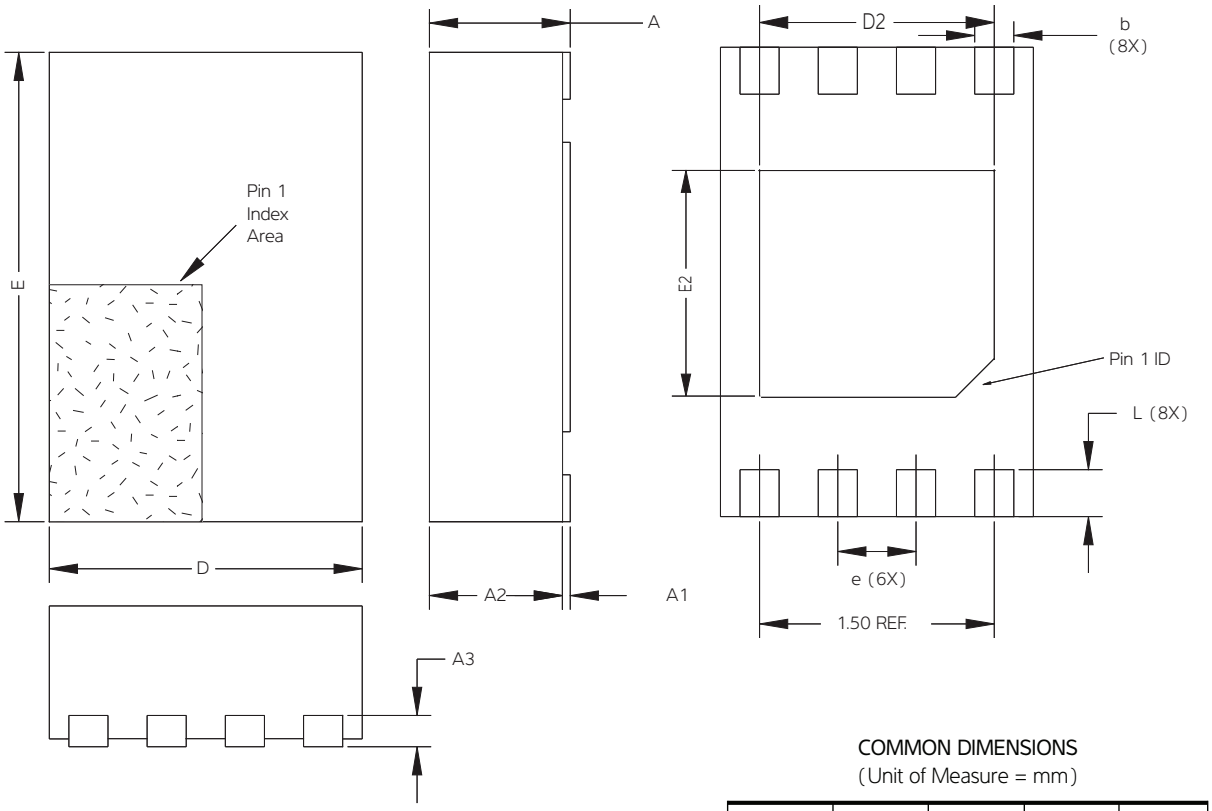
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/19/10

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8A2, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8A2	E

8Y6 – UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

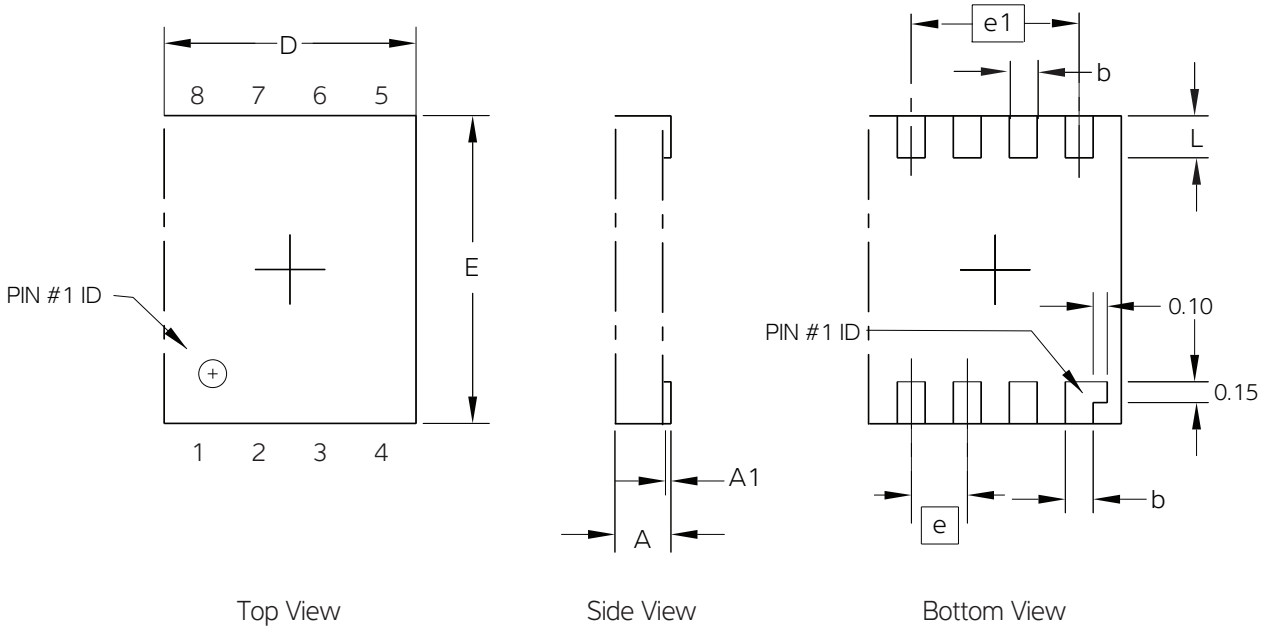
SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	–	–	1.40	
A	–	–	0.60	
A1	0.00	0.02	0.05	
A2	–	–	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

11/21/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8Y6**, 8-lead, 2.0x3.0mm Body, 0.50mm Pitch, UltraThin Mini-MAP, Dual No Lead Package (Sawn) (UDFN)	YNZ	8Y6	E

8ME1 – XDFN



Top View Side View Bottom View

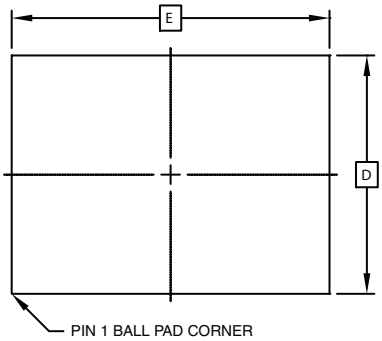
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e	0.40 TYP			
e1	1.20 REF			
L	0.26	0.30	0.35	

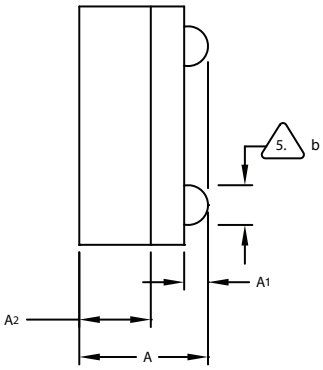
8/3/09

Package Drawing Contact: packagedrawings@atmel.com	TITLE 8ME1, 8-lead (1.80 x 2.20mm Body) Extra Thin DFN (XDFN)	GPC DTP	DRAWING NO. 8ME1	REV. A

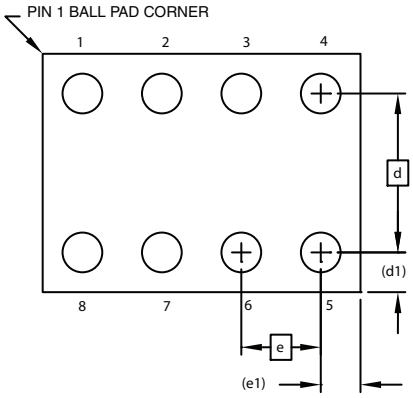
8U3-1 – VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW

8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D		1.50 BSC		
E		2.0 BSC		
e		0.50 BSC		
e1		0.25 REF		
d		1.00 BSC		
d1		0.25 REF		

07/14/10

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8U3-1, 8-ball, 1.50 x 2.00 mm Body, 0.50 pitch, VFBGA Package (dBGA2)	GXU	8U3-1	D

7. Revision History

Revision No.	Date	Comments
8735A	01/2011	Initial document release

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