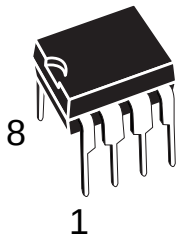
M35080

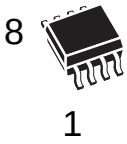
8 Kbit Serial SPI Bus EEPROM With Incremental Registers

PRELIMINARY DATA

- Compatible with SPI Bus Serial Interface (Positive Clock SPI Modes)
- Single Supply Voltage: 4.5 V to 5.5 V
- 5 MHz Clock Rate (maximum)
- Sixteen 16-bit Incremental Registers
- BYTE and PAGE WRITE (up to 32 Bytes) (except for the Incremental Registers)
- Self-Timed Programming Cycle
- Hardware Protection of the Status Register
- Resizeable Read-Only EEPROM Area
- Enhanced ESD Protection
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



PSDIP8 (BN)
0.25 mm frame



SO8 (MN)
150 mil width

DESCRIPTION

The M35080 device consists of 1024x8 bits of low power EEPROM, fabricated with STMicroelectronics' proprietary High Endurance Double Polysilicon CMOS technology.

The device is accessed by a simple SPI-compatible serial interface. The bus signals consist of a serial clock input (C), a serial data input (D) and a serial data output (Q), as shown in Table 1.

The device is selected when the chip select input ($\overline{S}$) is held low. Data is clocked in during the low to high transition of the clock, C. Data is clocked out during the high to low transition of the clock.

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

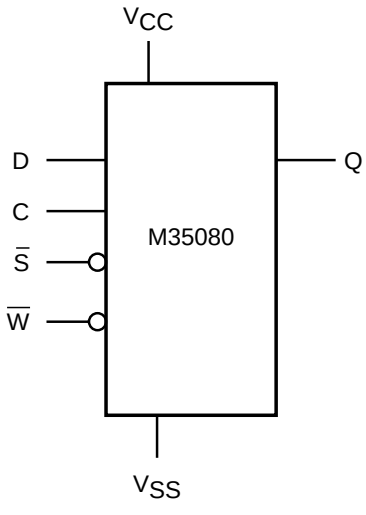
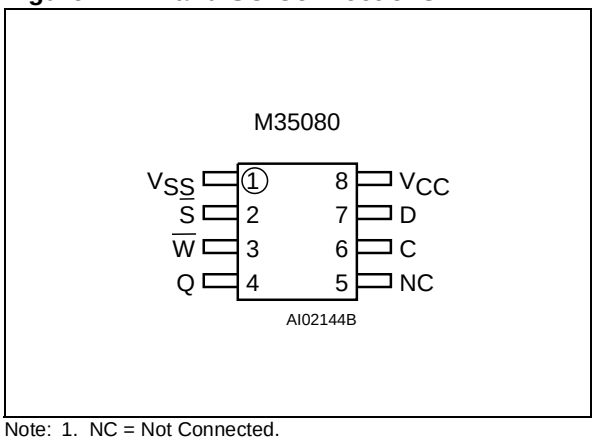


Figure 2. DIP and SO Connections



Note: 1. NC = Not Connected.

The memory is organized in pages of 32 bytes. However, the first page is not treated in the same way as the others. Instead, it is considered to consist of sixteen 16-bit incremental registers. Each register can be modified using the conventional write instructions, but the new value will only be accepted if it is greater than the current value. Thus, each register is restricted to being modified monotonically upwards.

This is useful in applications where it is necessary to implement a counter that is protected from fraudulent tampering (such as in a car odometer, an electricity meter, or a tally for remaining credit).

SIGNAL DESCRIPTION

Serial Output (Q)

The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D)

The input pin is used to transfer data serially into the device. Instructions, addresses, and the data to be written, are each received this way. Input is latched on the rising edge of the serial clock.

Serial Clock (C)

The serial clock provides the timing for the serial interface (as shown in Figure 3). Instructions, addresses, or data are latched, from the input pin, on the rising edge of the clock input. The output data on the Q pin changes state after the falling edge of the clock input.

Chip Select ($\overline{S}$)

When $\overline{S}$ is high, the memory device is deselected, and the Q output pin is held in its high impedance state. Unless an internal write operation is underway, the memory device is placed in its stand-by power mode.

After power-on, a high-to-low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$)

The protection features of the memory device are summarized in Table 3.

The hardware write protection, controlled by the $\overline{W}$ pin, restricts write access to the Status Register

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec	260 215	°C
V_O	Output Voltage Range		-0.3 to V_{CC}+0.6	V
V_I	Input Voltage Range		-0.3 to 6.5	V
V_{CC}	Supply Voltage Range		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V
	Electrostatic Discharge Voltage (Machine model) [3]		400	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500W).
3. EIAJ IC-121 (Condition C) (200pF, 0W).

Table 3. Write Protection Control

$\overline{W}$	SRWD Bit	Mode	Status Register	Data Bytes	
				Protected Area	Unprotected Area
0 or 1	0	Software Protected (SPM)	Writeable (if the WREN instruction has set the WEL bit)	Software write protected by the BP0 and BP1 bits of the status register	Writeable (if the WREN instruction has set the WEL bit)
1	1				
0	1	Hardware Protected (HPM)	Hardware write protected	Hardware write protected by the BP0 and BP1 bits of the status register	Writeable (if the WREN instruction has set the WEL bit)

(though not to the WIP and WEL bits, which are set or reset by the device's internal logic).

Bit 7 of the status register (as shown in Table 4) is the Status Register Write Disable bit (SRWD). When this is set to 0 (its initial delivery state) it is possible to write to the status register if the WEL bit (Write Enable Latch) has been set by the WREN instruction (irrespective of the level being applied to the $\overline{W}$ input).

When bit 7 (SRWD) of the status register is set to 1, the ability to write to the status register depends on the logic level being presented at pin $\overline{W}$:

– If $\overline{W}$ pin is high, it is possible to write to the status register, after having set the WEL bit using the WREN instruction (Write Enable Latch).

– If $\overline{W}$ pin is low, any attempt to modify the status register is ignored by the device, even if the WEL bit has been set. As a consequence, all the data bytes in the EEPROM area, protected by the BP1 and BP0 bits of the status register, are also hardware protected against data corruption, and appear as a Read Only EEPROM area for the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) either by setting the SRWD bit after pulling low the $\overline{W}$ pin, or by pulling low the $\overline{W}$ pin after setting the SRWD bit.

The only way to abort the Hardware Protected Mode, once entered, is to pull high the $\overline{W}$ pin.

If $\overline{W}$ pin is permanently tied to the high level, the Hardware Protected Mode is never activated, and the memory device only allows the user to protect a part of the memory, using the BP1 and BP0 bits of the status register, in the Software Protected Mode (SPM).

***IMPORTANT:** if $\overline{W}$ pin is left floating, not driven by the application, $\overline{W}$ is read as a logical '0'.*

Table 4. Status Register Format

b7							b0
SRWD	UV	X	INC	BP1	BP0	WEL	WIP

Note: 1. BP0, BP1: Read and write bits
2. UV, INC, WEL, WIP: Read only bits.
3. SRWD: Read and Write bit.

Figure 3. Data and Clock Timing

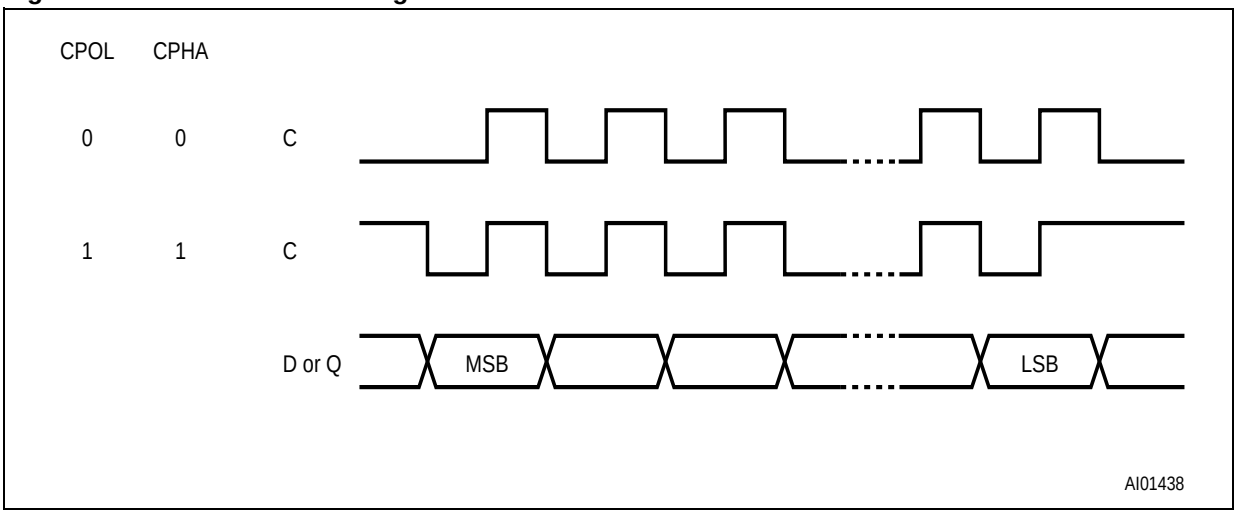
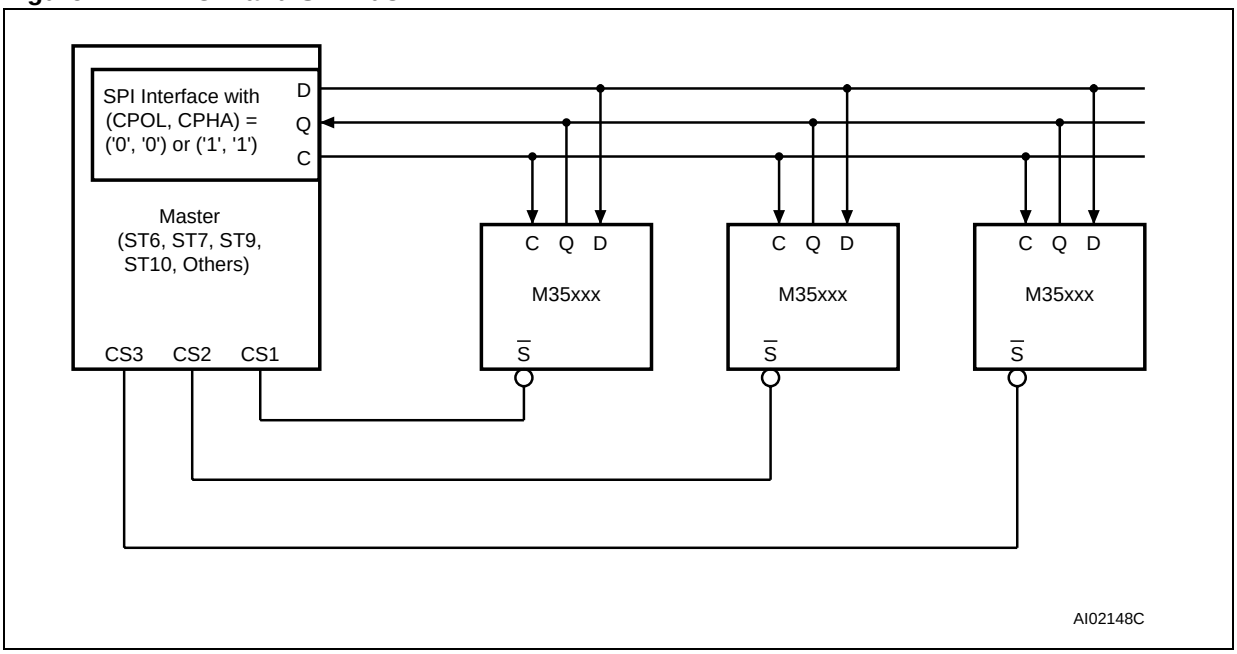


Figure 4. EEPROM and SPI Bus



OPERATIONS

All instructions, addresses and data are shifted serially in and out of the chip (along the bus, as shown in Figure 4). The most significant bit is presented first, with the data input (D) sampled on the first rising edge of the clock (C) after the chip select ($\overline{S}$) goes low (as shown in Figure 5, Figure 9, and Figure 12).

Every instruction, as summarized in Table 5, starts with a single-byte code. If an invalid instruction is sent (one not contained in Table 5), the chip automatically deselects itself.

The instruction code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the device must have been previously selected ($\overline{S}$ held low).

Protection of the First 32 Bytes

The first 32-byte page is organized as 16 words (two bytes each). The initial content of each word on this page is 0000h. When writing to byte-pair, a logic comparator verifies that the new two-byte value is larger than the value currently stored. If the new value is smaller than the current one, no operation is performed. It is impossible to write a value lower than the previous one, irrespective of the state of $\overline{W}$ pin and status register, as indicated in Table 6.

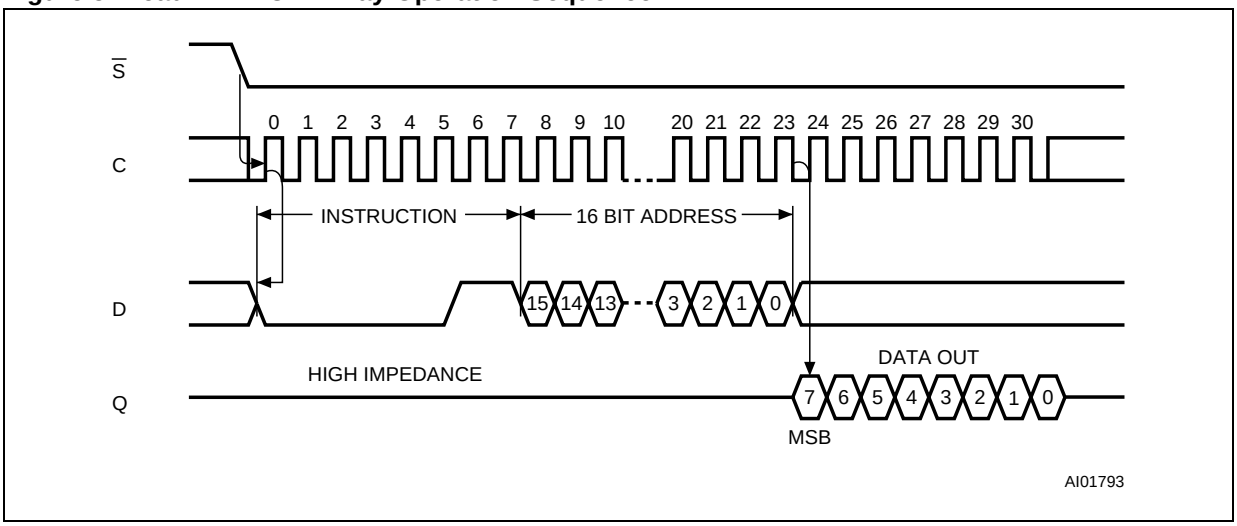
Write Enable (WREN) and Write Disable (WRDI)

The write enable latch, inside the memory device, must be set prior to each WRITE and WRSR operation. The WREN instruction (write enable) sets this latch, and the WRDI instruction (write disable) resets it.

Table 5. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010
WRINC	Write Data to Secure Array	0000 0111

Figure 5. Read EEPROM Array Operation Sequence



Note: 1. The most significant address bits, A15-A10, are treated as Don't Care.

The latch becomes reset by any of the following events:

– Power on
– WRDI instruction completion
– WRSR instruction completion
– WRITE instruction completion.

As soon as the WREN or WRDI instruction is received, the memory device first executes the instruction, then enters a wait mode until the device is deselected.

Read Status Register (RDSR)

The RDSR instruction allows the status register to be read, and can be sent at any time, even during a Write operation. Indeed, when a Write is in progress, it is recommended that the value of the Write-In-Progress (WIP) bit be checked. The value in the WIP bit (whose position in the status register is shown in Table 4) can be continuously polled, before sending a new WRITE instruction. This can be performed in one of two ways:

- Repeated RDSR instructions (each one consisting of $\overline{S}$ being taken low, C being clocked 8 times for the instruction and 8 times for the read operation, and $\overline{S}$ being taken high)
- A single, prolonged RDSR instruction (consisting of $\overline{S}$ being taken low, C being clocked 8 times for the instruction and kept running for repeated read operations), as shown in Figure 6.

The Write-In-Process (WIP) bit is read-only, and indicates whether the memory is busy with a Write operation. A '1' indicates that a write is in progress, and a '0' that no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. It, too, is read-only. Its value can only be changed by one of the events listed earlier, or as a result of executing WREN or WRDI instruction. It cannot be changed using a WRSR instruction. A '1' indicates that the latch is set (the forthcoming Write instruction will be executed), and a '0' that it is reset (and any forthcoming Write instructions will be ignored).

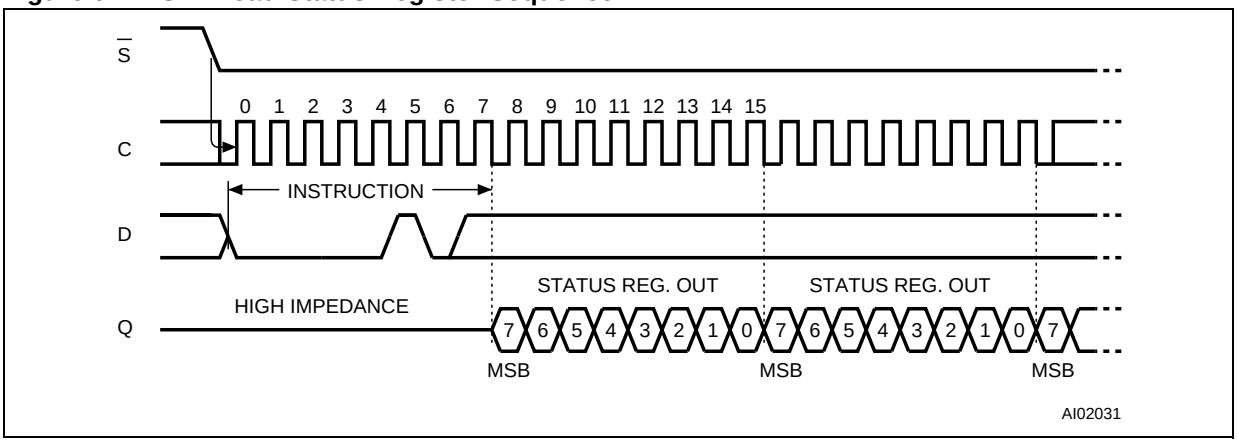
The Block Protect (BP0 and BP1) bits indicate the amount of the memory that is to be write-protected. These two bits are non-volatile. They are set using a WRSR instruction.

During a Write operation (whether it be to the memory area or to the status register), all bits of the status register remain valid, and can be read using the RDSR instruction. However, during a Write operation, the values of the non-volatile bits

Table 6. Memory Mapping

Address	Protection
000h-01Fh	Incremental area: a word (2 bytes) can be written only if the new value to write is larger than the value already stored
020h-3FFh	No specific protection except the one as of Table 7

Figure 6. RDSR: Read Status Register Sequence



(SRWD, BP0, BP1) become frozen at a constant value. The updated value of these bits becomes available when a new RDSR instruction is executed, after completion of the write cycle. On the other hand, the two read-only bits (WEL, WIP) are dynamically updated during internal write cycles. Using this facility, it is possible to poll the WIP bit to detect the end of the internal write cycle.

The Comparator bit (INC) indicates if the new value written in the 16 first word is lower '1' or higher '0' than the previous stored value.

The UV bit indicates if the memory chip has been erased.

Write Status Register (WRSR)

The format of the WRSR instruction is shown in Figure 7. After the instruction and the eight bits of the status register have been latched-in, the internal Write cycle is triggered by the rising edge of the $\overline{S}$ line. This must occur after the falling edge of the 16th clock pulse, and before the rising edge of the 17th clock (as indicated in Figure 7), otherwise the internal write sequence is not performed.

The WRSR instruction is used for the following:

- to select the size of memory area that is to be write-protected
- to select between SPM (Software Protected Mode) and HPM (Hardware Protected Mode).

The size of the write-protection area applies equally in SPM and HPM. The BP1 and BP0 bits of the status register have the appropriate value (see Table 7) written into them after the contents of the protected area of the EEPROM have been written.

The initial delivery state of the BP1 and BP0 bits is 00, indicating a write-protection size of 0.

Figure 7. WRSR: Write Status Register Sequence

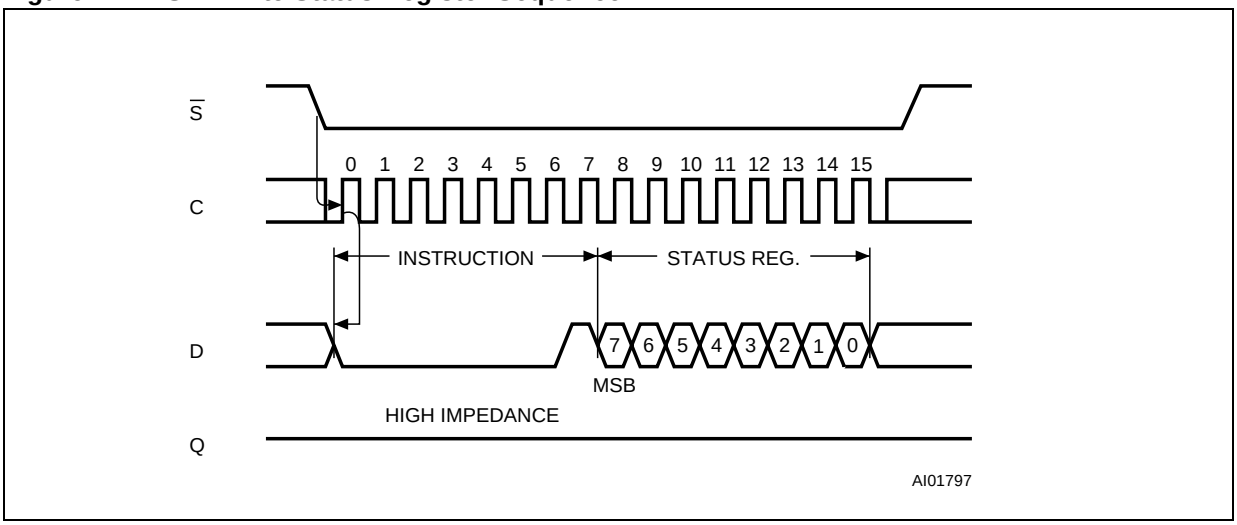


Table 7. Write Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected
BP1	BP0		M35080
0	0	none [1]	none [1]
0	1	Upper quarter	0300h - 03FFh
1	0	Upper half	0200h - 03FFh

Note: 1. Except for the first sixteen pairs of bytes (see Table 6).

Software Protected Mode (SPM)

The act of writing a non-zero value to the BP1 and BP0 bits causes the Software Protected Mode (SPM) to be started. All attempts to write a byte or page in the protected area are ignored, even if the Write Enable Latch is set. However, writing is still allowed in the unprotected area of the memory array and to the SRWD, BP1 and BP0 bits of the status register, provided that the WEL bit is first set.

Hardware Protected Mode (HPM)

The Hardware Protected Mode (HPM) offers a higher level of protection, and can be selected by setting the SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting the SRWD bit. The SRWD is set by the WSR instruction, provided that the WEL bit is first set. The setting of the SRWD bit can be made independently of, or at the same time as, writing a new value to the BP1 and BP0 bits.

Once the device is in the Hardware Protected Mode, the data bytes in the protected area of the memory array, *and* the content of the status register, are write-protected. The only way to re-enable writing new values to the status register is to pull the $\overline{W}$ pin high. This cause the device to leave the Hardware Protected Mode, and to revert to being in the Software Protected Mode. (The value in the BP1 and BP0 bits will not have been changed).

Further details of the operation of the Write Protect pin ($\overline{W}$) are given earlier, on page 2.

Typical Use of HPM and SPM

The $\overline{W}$ pin can be dynamically driven by an output port of a microcontroller. It is also possible, though, to connect it permanently to V_{SS} (by a solder connection, or through a pull-down resistor). The manufacturer of such a printed circuit board can take the memory device, still in its initial delivery state, and can solder it directly on to the board. After power on, the microcontroller can be instructed to write the protected data into the appropriate area of the memory. When it has finished, the appropriate values are written to the BP1, BP0 and SRWD bits, thereby putting the device in the hardware protected mode.

An alternative method is to write the protected data, and to set the BP1, BP0 and SRWD bits, before soldering the memory device to the board. Again, this results in the memory device being placed in its hardware protected mode.

If the $\overline{W}$ pin has been connected to V_{SS} by a pull-down resistor, the memory device can be taken out of the hardware protected mode by driving the $\overline{W}$ pin high, to override the pull-down resistor.

If the $\overline{W}$ pin has been directly soldered to V_{SS}, there is only one way of taking the memory device out of the hardware protected mode: the memory device must be de-soldered from the board, and connected to external equipment in which the $\overline{W}$ pin is allowed to be taken high.

Read Operation

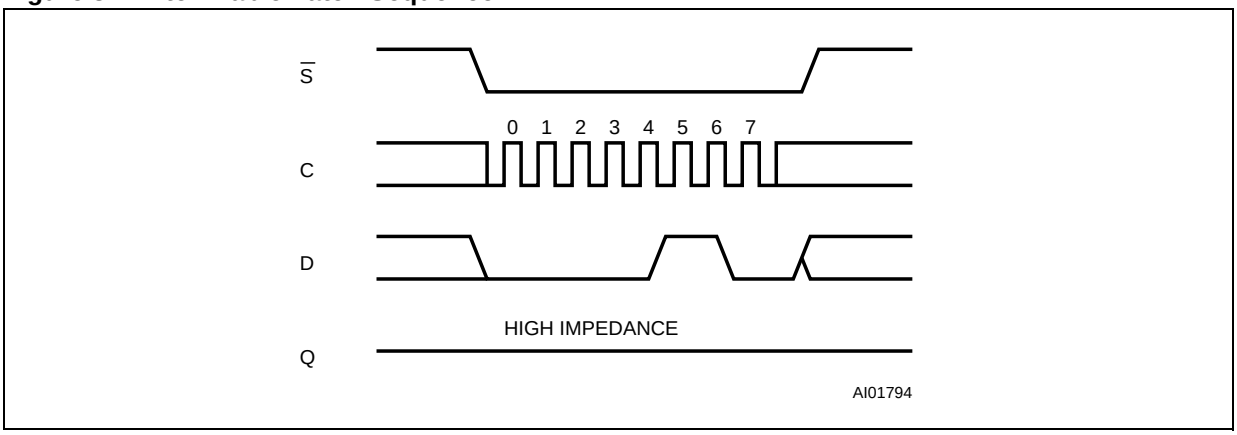
The chip is first selected by holding $\overline{S}$ low. The serial one byte read instruction is followed by a two byte address (A15-A0), each bit being latched-in during the rising edge of the clock (C). The data stored in the memory, at the selected address, is shifted out on the Q output pin. Each bit is shifted out during the falling edge of the clock (C) as shown in Figure 5.

The internal address counter is automatically incremented to the next higher address after each byte of data has been shifted out. The data stored in the memory, at the next address, can be read by successive clock pulses. When the highest address is reached, the address counter rolls over to “0000h”, allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. If a read instruction is received during a write cycle, it is rejected, and the memory device deselects itself.

Byte Write Operation

Before any write can take place, the WEL bit must be set, using the WREN instruction, as shown in Figure 8. The write state is entered by selecting the chip, issuing three bytes of instruction and address, and one byte of data. Chip Select ($\overline{S}$) must remain low throughout the operation, as shown in Figure 9. The device must be deselected just after the eighth bit of the data byte has been latched in,

Figure 8. Write Enable Latch Sequence



as shown in Figure 9, otherwise the write process is cancelled. As soon as the memory device is deselected, the self-timed internal write cycle is initiated. While the write is in progress, the status register may be read to check the status of the SRWD, BP1, BP0, WEL and WIP bits. In particular, WIP contains a '1' during the self-timed write cycle, and a '0' when the cycle is complete, (at which point the write enable latch is also reset).

Write Data In the Incremental Registers

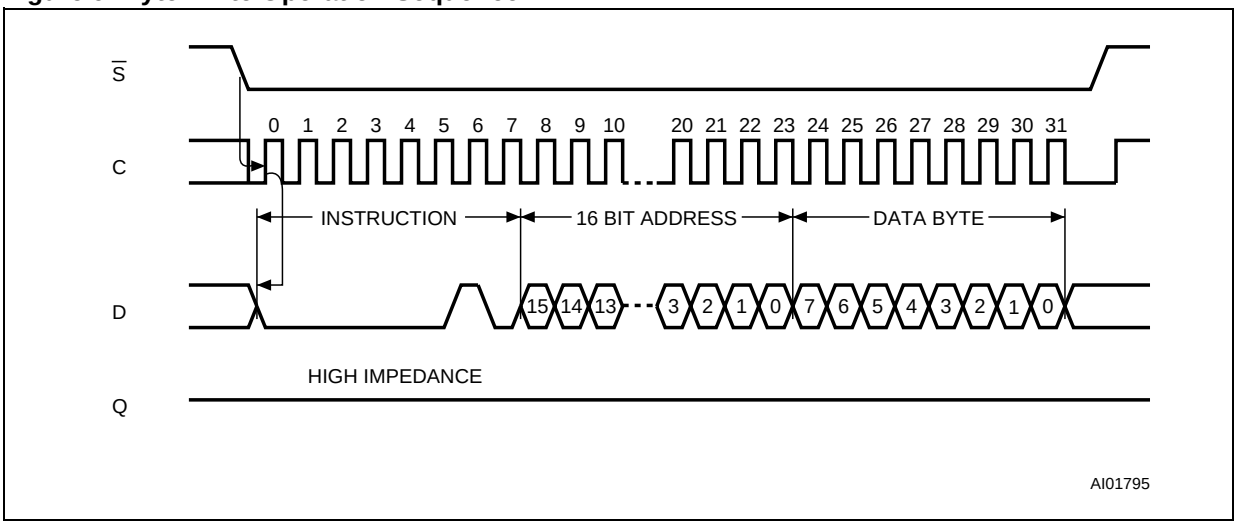
Due to the special control on the first page of the memory, the byte write operation is not usable on the first 32 bytes. Instead, the WRINC instruction must be used, the timing of which is shown in Figure 10.

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected (by taking $\overline{S}$ low) and a serial WREN instruction is issued. Then the device is deselected, by taking $\overline{S}$ high for at least t_{SHSL}. The device sets the write enable latch, and remains in its stand-by state, until it is deselected. Then the write state is entered by selecting the chip, by taking $\overline{S}$ low. The WRINC instruction is issued, and the address is sent (always an even address, with A0=0) along with two bytes of data. The Chip Select input ($\overline{S}$) must remain low for the entire duration of the operation.

The device must be deselected just after the eighth bit of the second data byte has been latched in. Otherwise, the write process is cancelled. As a further protection, the WRINC instruction is cancelled if its duration is not exactly equal to 40 clock pulses.

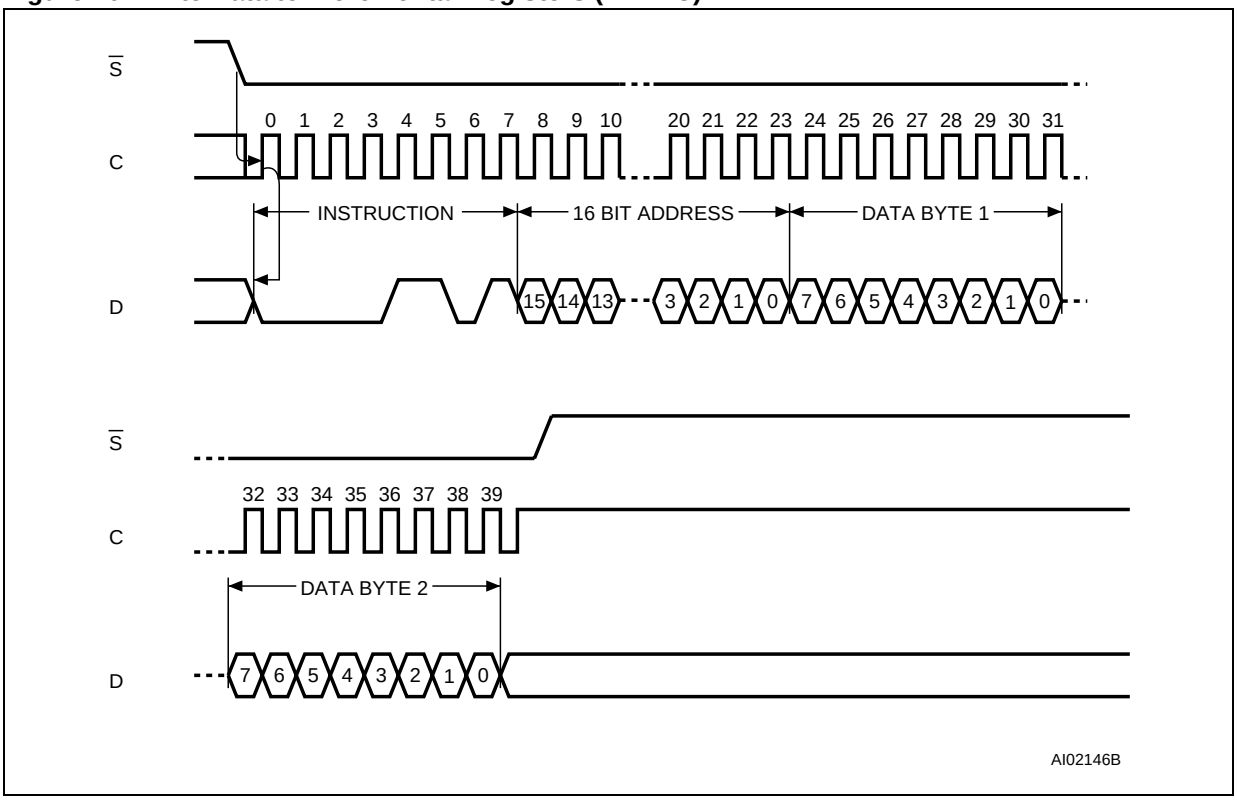
As soon as the device is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read, to check the values of the UV, INC, BP1, BP0, WEL and

Figure 9. Byte Write Operation Sequence



Note: 1. The most significant address bits, A15-A10, are treated as Don't Care.

Figure 10. Write Data to Incremental Registers (WRINC)



Note: 1. The most significant address bits, A15-A10, are treated as Don't Care.

WIP bits. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 32 bytes of data can be written during one Write time, t_W, provided that they are all to the same page (see Figure 11). The Page Write operation is the same as the Byte Write operation, except that instead of deselecting the device after the first byte of data, up to 31 additional bytes can be shifted in (and the device is deselected after the last byte).

Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (an address of the form xxxx xxxx xxx1 1111) and the clock continues, the counter rolls over to the first address of the same page (xxxx xxxx xxx0 0000) and overwrites any previously written data.

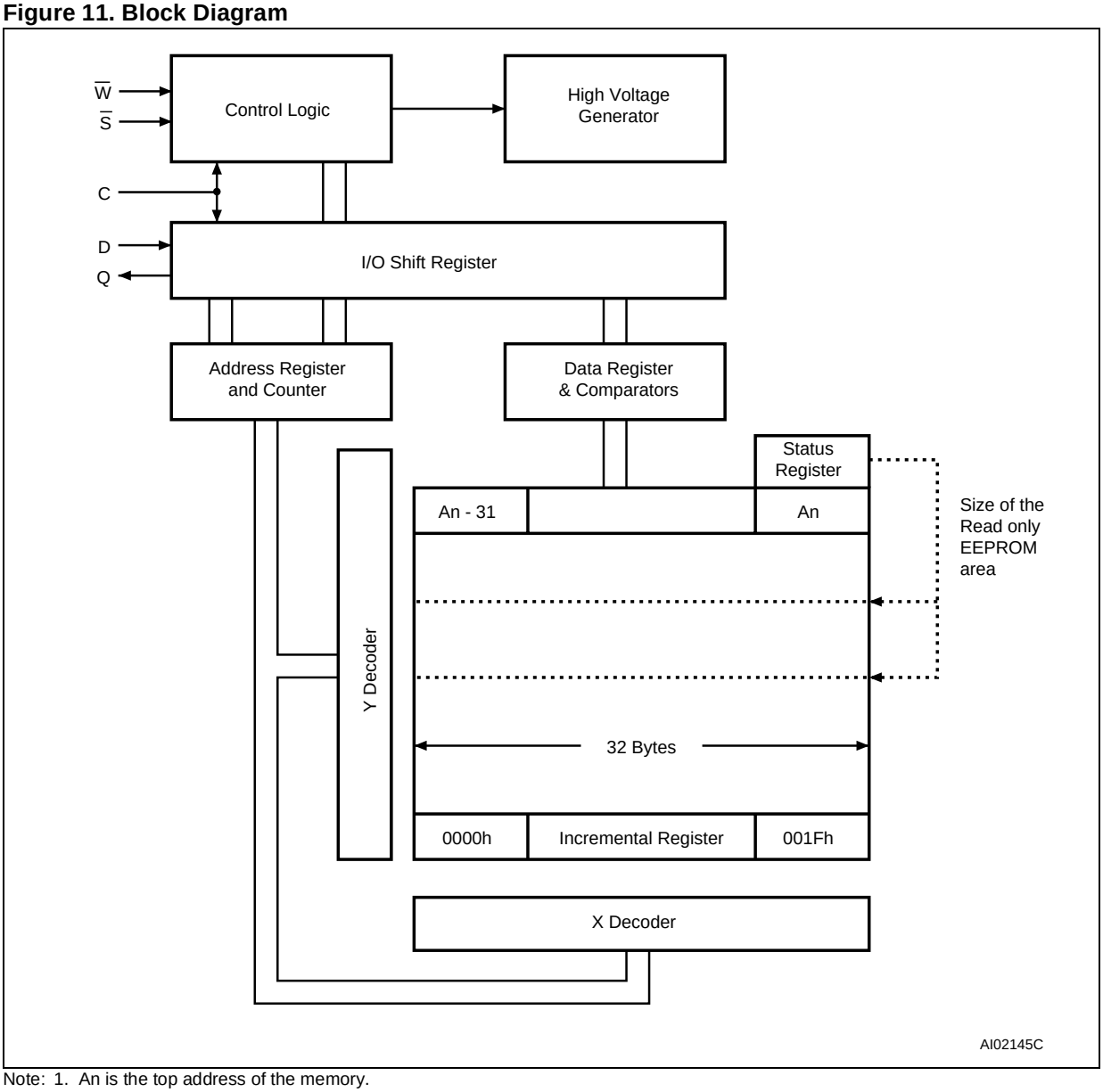
As before, the Write cycle only starts if the $\overline{S}$ transition occurs just after the eighth bit of the last data byte has been received, as shown in Figure 12.

DATA PROTECTION AND PROTOCOL SAFETY

To protect the data in the memory from inadvertent corruption, the memory device only responds to correctly formulated commands. The main security measures can be summarized as follows:

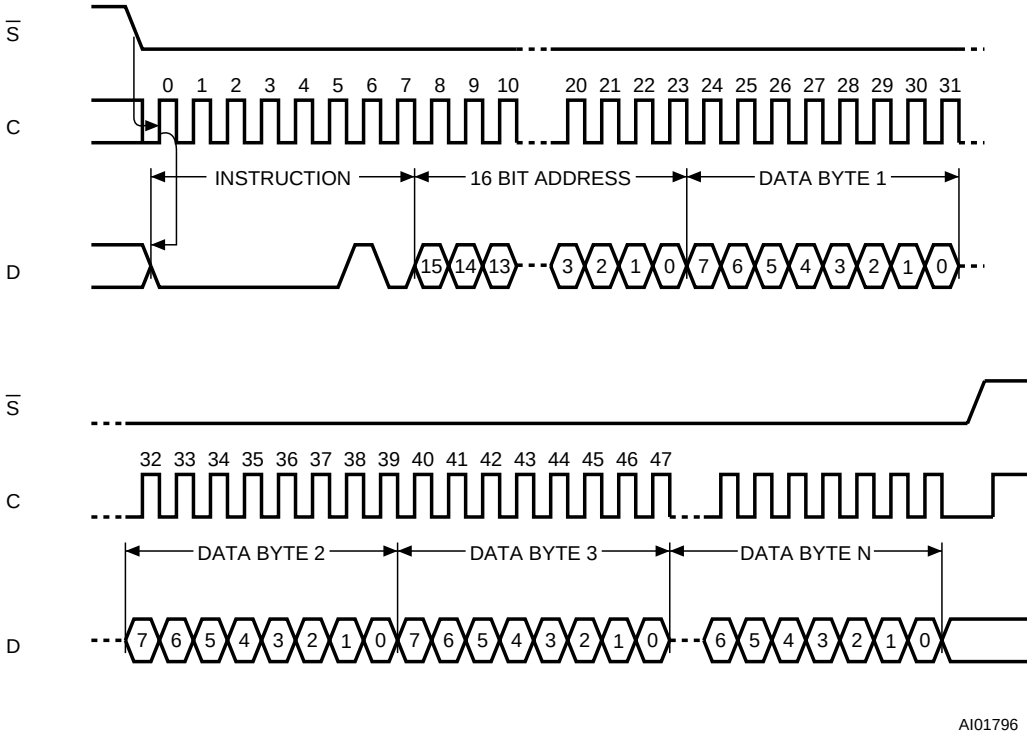
- The WEL bit is reset at power-up.
- $\overline{S}$ must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile write cycle (in the memory array or in the status register).
- Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
- After execution of a WREN, WRDI, or RDSR instruction, the device enters a wait state, and waits to be deselected.
- Invalid $\overline{S}$ transitions are ignored.

Figure 11. Block Diagram



Note: 1. An is the top address of the memory.

Figure 12. Page Write Operation Sequence



Note: 1. The most significant address bits, A15-A10, are treated as Don't Care.
2. The number of clock pulses must be a multiple of 8. Otherwise, the write is aborted.

POWER ON STATE

After power-on, the memory device is in the following state:

- low power stand-by state
- deselected (after power-on, a high-to-low transition is required on the $\overline{S}$ input before any operations can be started).
- the WEL bit is reset
- the SRWD, BP1 and BP0 bits of the status register are unchanged from the previous power-down (they are non-volatile bits).

Table 8. Initial Status Register Format

b7							b0
0	0	0	1	0	0	0	0

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state. With the exception of the first 32 bytes, all data bits are set to '1', and hence all data bytes are at FFh. The first 32 bytes are set to all '0's, and hence the first 16 words at 0000h.

The status register bits are initialized to '0', except for bit b4, which is set to '1', as shown in Table 8.

Table 9. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, @ 5 MHz, V_{CC} = 5V, Q = Open		3	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, @ 2 MHz, V_{CC} = 5V, Q = Open, Note 2		3	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		10	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		20	µA
V_{IL}	Input Low Voltage		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} 1	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
V_{OH} 1	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, Grade 3.

Table 10. Input Parameters 1
(T_A = 25 C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 11. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}
Output Load	C_L = 100pF

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output

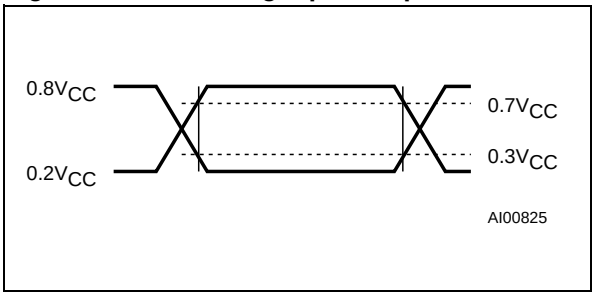


Table 12. AC Characteristics

Symbol	Alt.	Parameter	M35080				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2.1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	100		100		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	100		100		ns
t_{CH} (1)	t_{CLH}	Clock High Time	60		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	80		200		ns
t_{CLCH}	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL}	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		60		ns
t_{DLDH}	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL}	t_{FI}	Data In Fall Time		1		1	µs
t_{CHSH}		$\overline{S}$ Active Hold Time	200		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	100		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	200		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time		100		150	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		300	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		100	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production.

Figure 14. Serial Input Timing

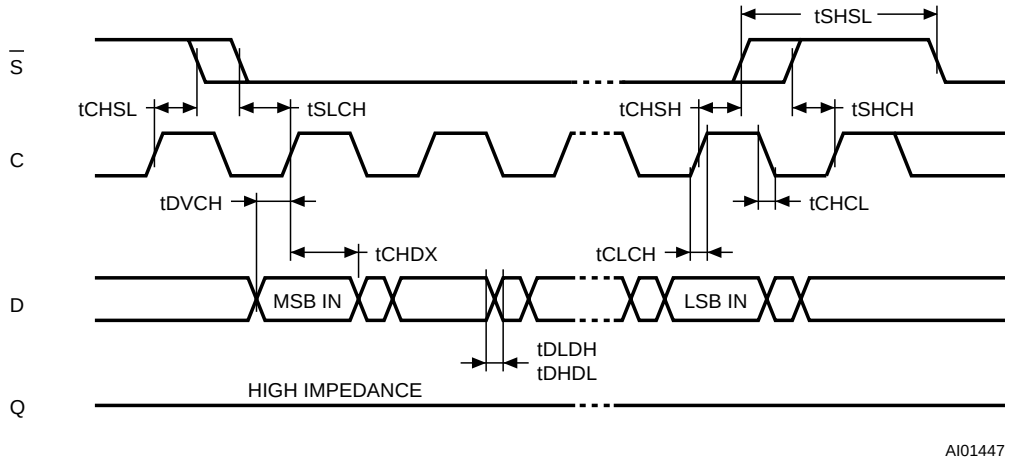
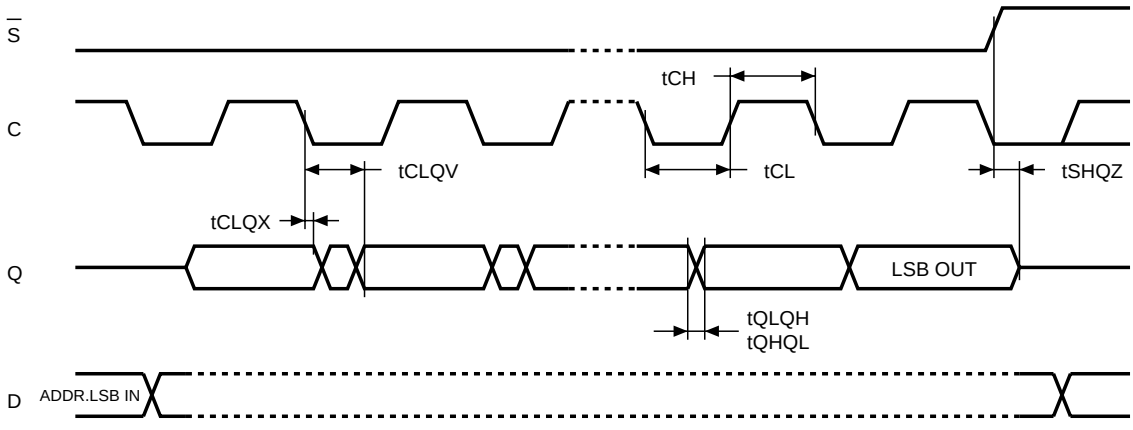


Figure 15. Output Timing



ORDERING INFORMATION

The notation used for the device number is as shown in Table 13. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 13. Ordering Information Scheme

Example: M35080 – MN 6 T

Package	
BN	PSDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)

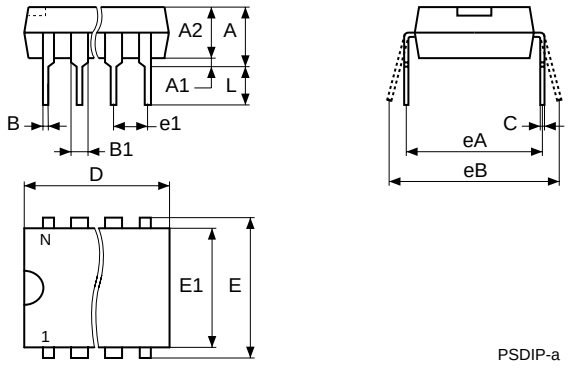
Temperature Range	
6	–40 °C to 85 °C
3	–40 °C to 125 °C

Option	
T	Tape and Reel Packing

Table 14. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 16. PSDIP8 (BN)

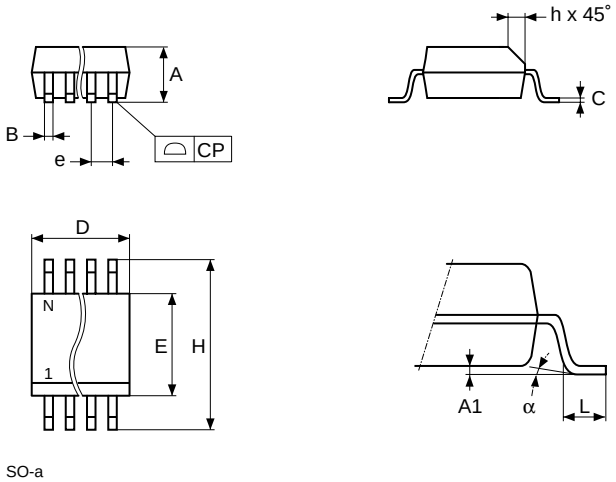


Note: 1. Drawing is not to scale.

Table 15. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 17. SO8 narrow (MN)



SO-a

Note: 1. Drawing is not to scale.